



HMC617LP3 / 617LP3E

GaAs SMT PHEMT LOW NOISE AMPLIFIER, 0.55 - 1.2 GHz

Typical Applications

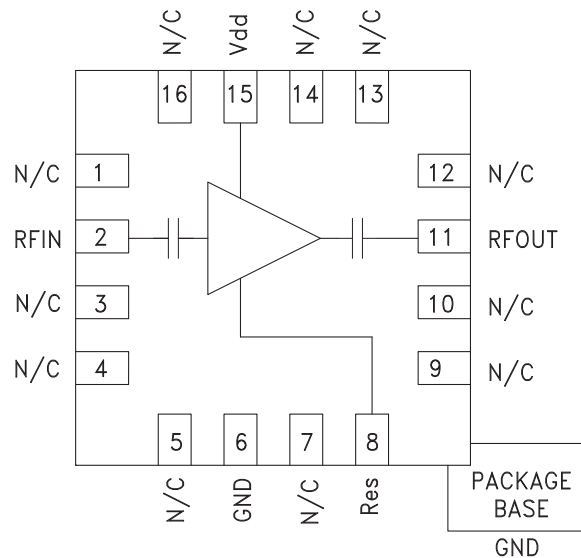
The HMC617LP3(E) is ideal for:

- Cellular/3G and LTE/WiMAX/4G
- BTS & Infrastructure
- Repeaters and Femtocells
- Public Safety Radio
- Access Points

Features

- Noise Figure: 0.5 dB
- Gain: 16 dB
- Output IP3: +37 dBm
- Single Supply: +3V to +5V
- 50 Ohm Matched Input/Output
- 16 Lead 3x3mm QFN Package: 9 mm²

Functional Diagram



General Description

The HMC617LP3(E) is a GaAs PHEMT MMIC Low Noise Amplifier that is ideal for Cellular/3G and LTE/WiMAX/4G basestation front-end receivers operating between 550 and 1200 MHz. The amplifier has been optimized to provide 0.5 dB noise figure, 16 dB gain and +37 dBm output IP3 from a single supply of +5V. Input and output return losses are excellent and the LNA requires minimal external matching and bias decoupling components. The HMC617LP3(E) shares the same package and pinout with the HMC618LP3(E) 1.7 - 2.2 GHz LNA. The HMC617LP3(E) can be biased with +3V to +5V and features an externally adjustable supply current which allows the designer to tailor the linearity performance of the LNA for each application. The HMC617LP3(E) offers improved noise figure versus the previously released HMC372LP3(E) and the HMC376LP3(E).

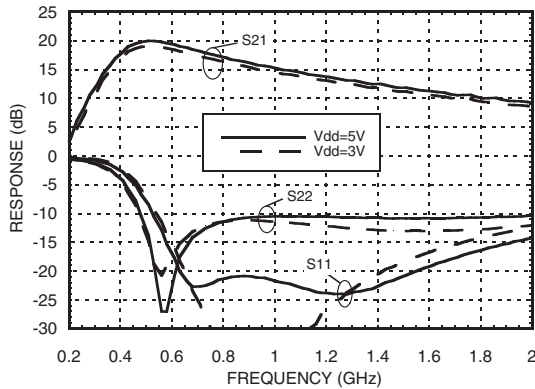
Electrical Specifications, $T_A = +25^\circ C$, $R_{bias} = 3.92k\ Ohms^*$

| Parameter | Vdd = +3 Vdc | | | | | | Vdd = +5 Vdc | | | | | | Units |
|--|--------------|-------|------|------------|-------|------|--------------|-------|------|------------|-------|------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Frequency Range | 698 - 960 | | | 550 - 1200 | | | 698 - 960 | | | 550 - 1200 | | | MHz |
| Gain | 13 | 16 | | 11 | 15 | | 13.5 | 16 | | 11.5 | 16 | | dB |
| Gain Variation Over Temperature | | 0.003 | | | 0.003 | | | 0.005 | | | 0.005 | | dB/°C |
| Noise Figure | | 0.5 | 0.8 | | 0.5 | 1.1 | | 0.55 | 0.85 | | 0.6 | 1.1 | dB |
| Input Return Loss | | 28 | | | 22 | | | 22 | | | 17 | | dB |
| Output Return Loss | | 12 | | | 14 | | | 12 | | | 15 | | dB |
| Output Power for 1 dB Compression (P1dB) | 14 | 16 | | 12.5 | 16 | | 18.5 | 21 | | 16.5 | 20 | | dBm |
| Saturated Output Power (Psat) | | 17 | | | 16.5 | | | 21 | | | 20.5 | | dBm |
| Output Third Order Intercept (IP3) | | 31 | | | 30 | | | 37 | | | 37 | | dBm |
| Supply Current (Idd) | | 30 | 45 | | 30 | 45 | | 88 | 115 | | 88 | 115 | mA |

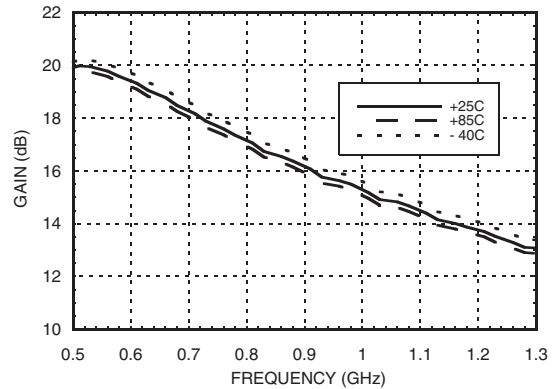
* Rbias resistor sets current, see application circuit herein



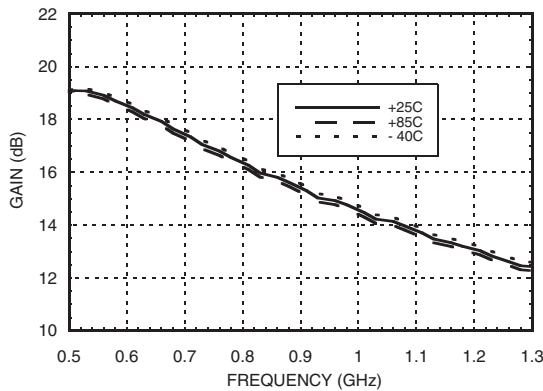
Broadband Gain & Return Loss [1] [2]



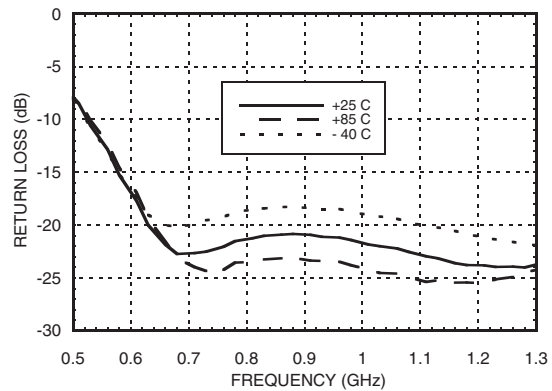
Gain vs. Temperature [1]



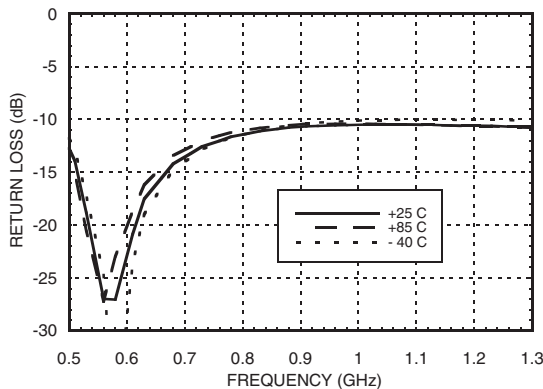
Gain vs. Temperature [2]



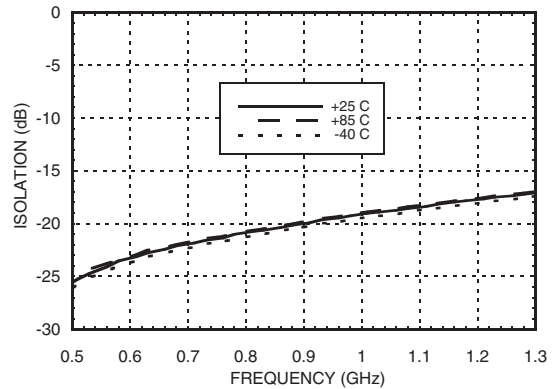
Input Return Loss vs. Temperature [1]



Output Return Loss vs. Temperature [1]

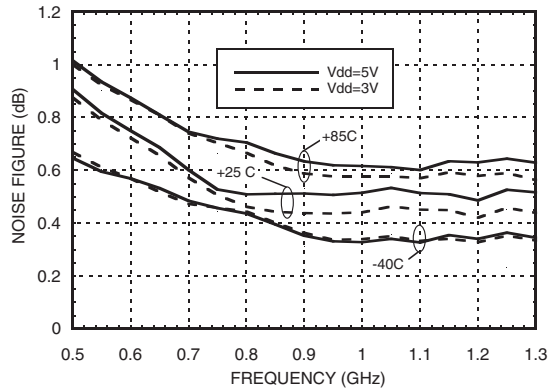


Reverse Isolation vs. Temperature [1]

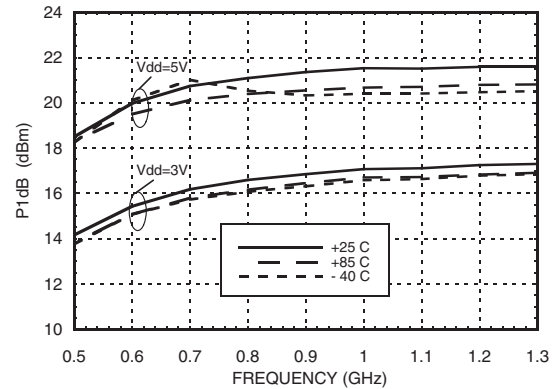


[1] Vdd = 5V, Rbias = 3.92K [2] Vdd = 3V, Rbias = 3.92K

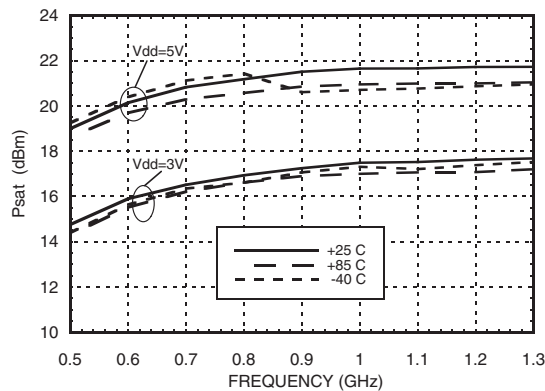
Noise Figure vs. Temperature [1] [2] [4]



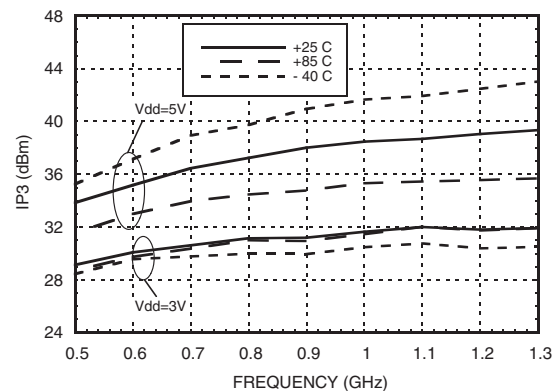
P1dB vs. Temperature [1] [2]



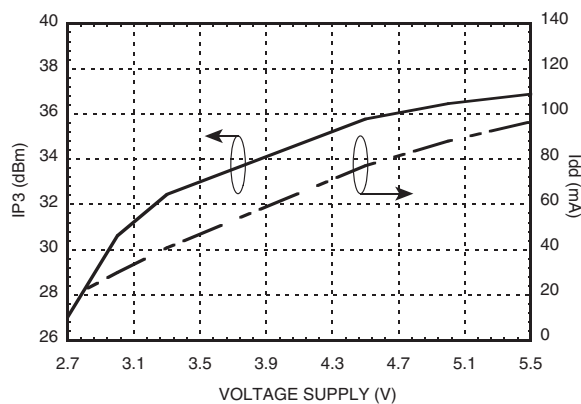
Psat vs. Temperature [1] [2]



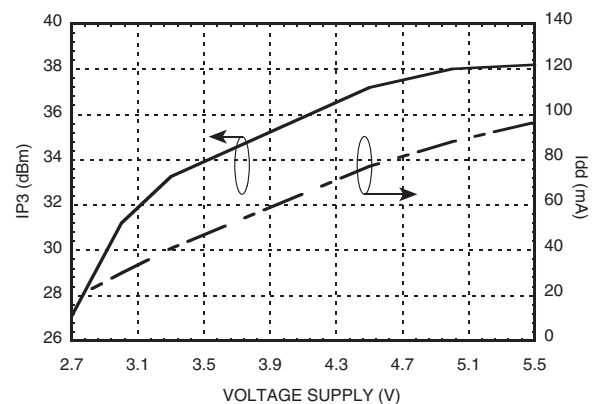
Output IP3 vs. Temperature [1] [2]



Output IP3 and I_{dd} vs. Supply Voltage @ 700 MHz [3]



Output IP3 and I_{dd} vs. Supply Voltage @ 900 MHz [3]

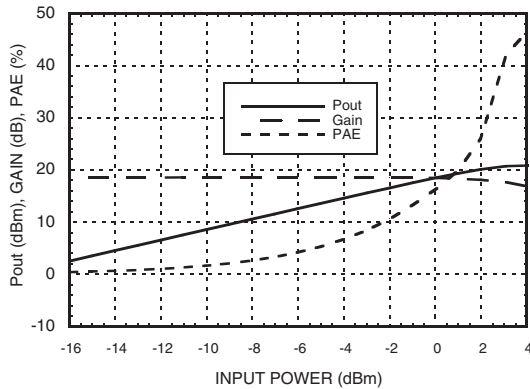


[1] V_{dd} = 5V, R_{bias} = 3.92K [2] V_{dd} = 3V, R_{bias} = 3.92K

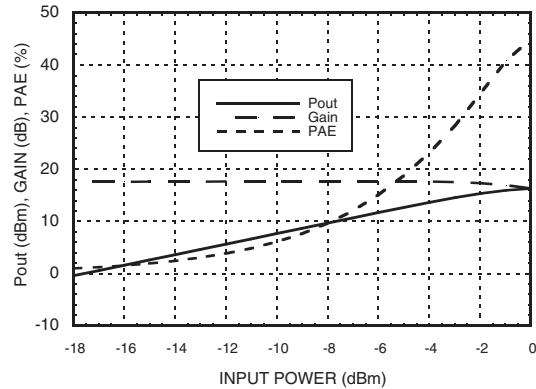
[3] R_{bias} = 3.92K [4] Measurement reference plane shown on evaluation PCB drawing.



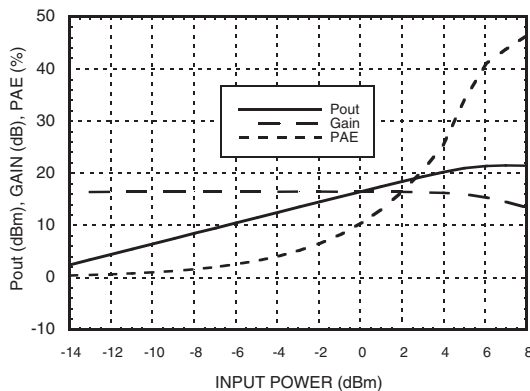
Power Compression @ 700 MHz [1]



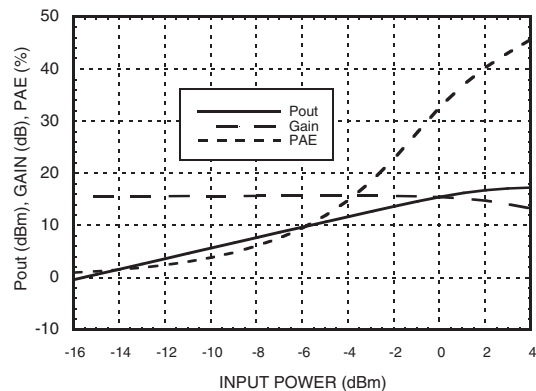
Power Compression @ 700 MHz [2]



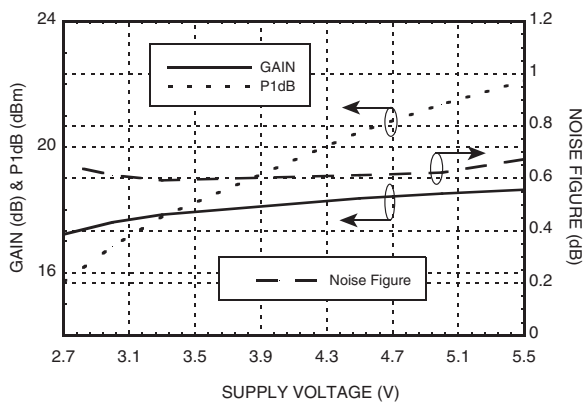
Power Compression @ 900 MHz [1]



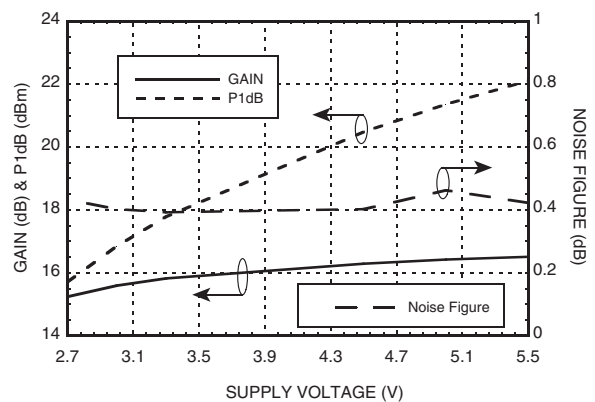
Power Compression @ 900 MHz [2]



**Gain, Power & Noise Figure
vs. Supply Voltage @ 700 MHz [3]**

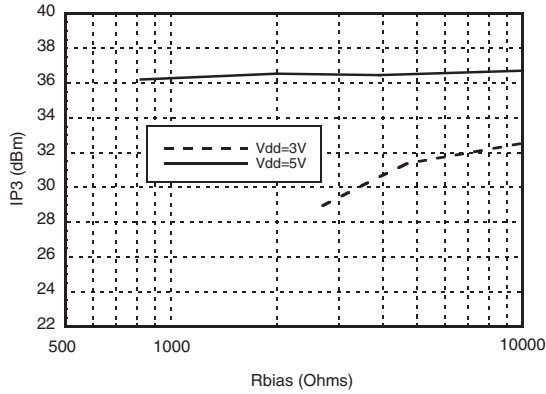


**Gain, Power & Noise Figure
vs. Supply Voltage @ 900 MHz [3]**

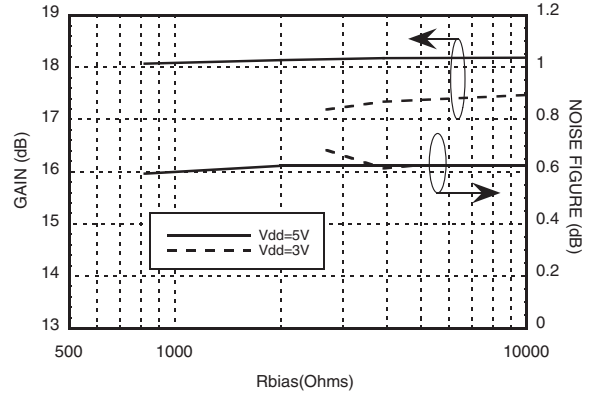


[1] Vdd = 5V, Rbias = 3.92K [2] Vdd = 3V, Rbias = 3.92K [3] Rbias = 3.92K

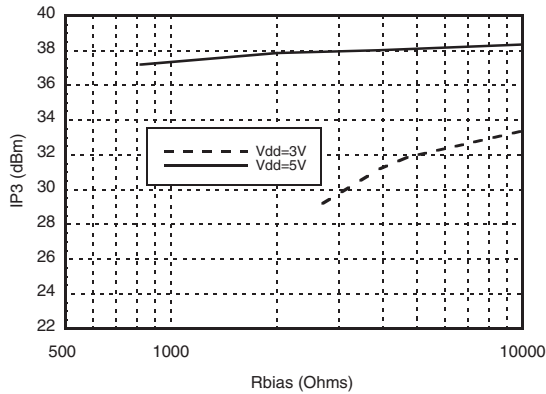
Output IP3 vs. Rbias @ 700 MHz



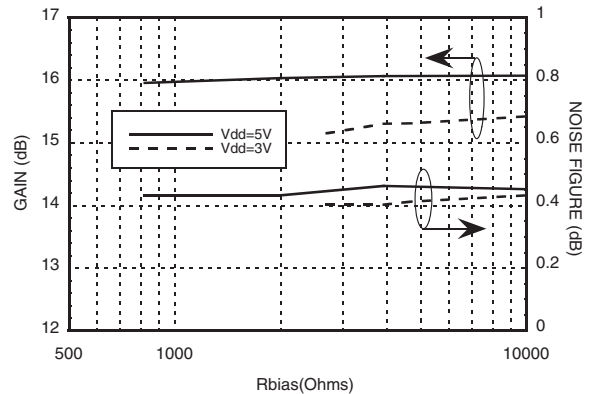
Gain, Noise Figure & Rbias @ 700 MHz



Output IP3 vs. Rbias @ 900 MHz



Gain, Noise Figure & Rbias @ 900 MHz



Absolute Bias Resistor

Range & Recommended Bias Resistor Values for Idd

| Vdd (V) | Rbias | | | Idd (mA) |
|---------|--------|--------------|-------------|----------|
| | Min | Max | Recommended | |
| 3V | 1K [1] | Open Circuit | 2.7k | 24 |
| | | | 3.92k | 30 |
| | | | 4.7k | 33 |
| | | | 10k | 40 |
| 5V | 0 | Open Circuit | 820 | 65 |
| | | | 2k | 78 |
| | | | 3.92k | 88 |
| | | | 10k | 90 |

[1] With Vdd= 3V and Rbias < 1K Ohm may result in the part becoming conditionally stable which is not recommended.

Absolute Maximum Ratings

| | |
|--|----------------|
| Drain Bias Voltage (Vdd) | +6V |
| RF Input Power (RFIN) (Vdd = +5 Vdc) | +10 dBm |
| Channel Temperature | 150 °C |
| Continuous Pdiss (T= 85 °C) (derate 8.33 mW/°C above 85 °C) | 0.54 W |
| Thermal Resistance (channel to ground paddle) | 120 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |

Typical Supply Current vs. Vdd (Rbias = 3.92k)

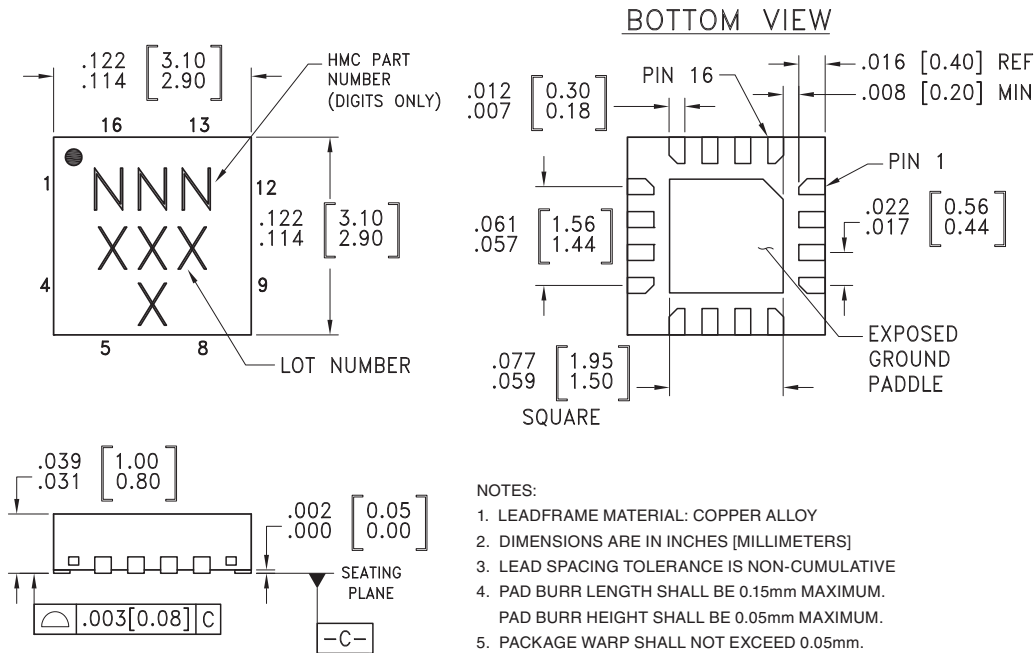
| Vdd (V) | Idd (mA) |
|---------|----------|
| 2.7 | 18 |
| 3.0 | 30 |
| 3.3 | 41 |
| 4.5 | 77 |
| 5.0 | 88 |
| 5.5 | 97 |

Note: Amplifier will operate over full voltage ranges shown above.



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

Outline Drawing



Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[3] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC617LP3 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 ^[1] | 617 XXXX |
| HMC617LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 ^[2] | 617 XXXX |

[1] Max peak reflow temperature of 235 °C

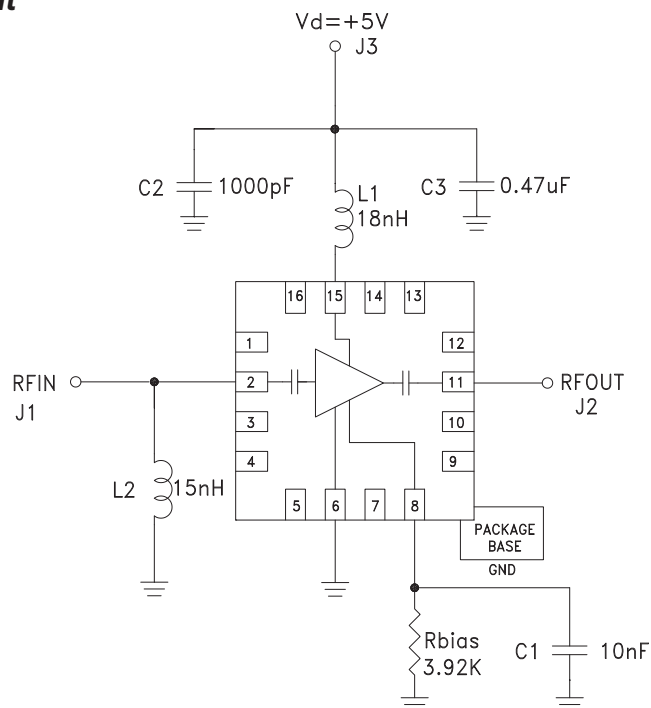
[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

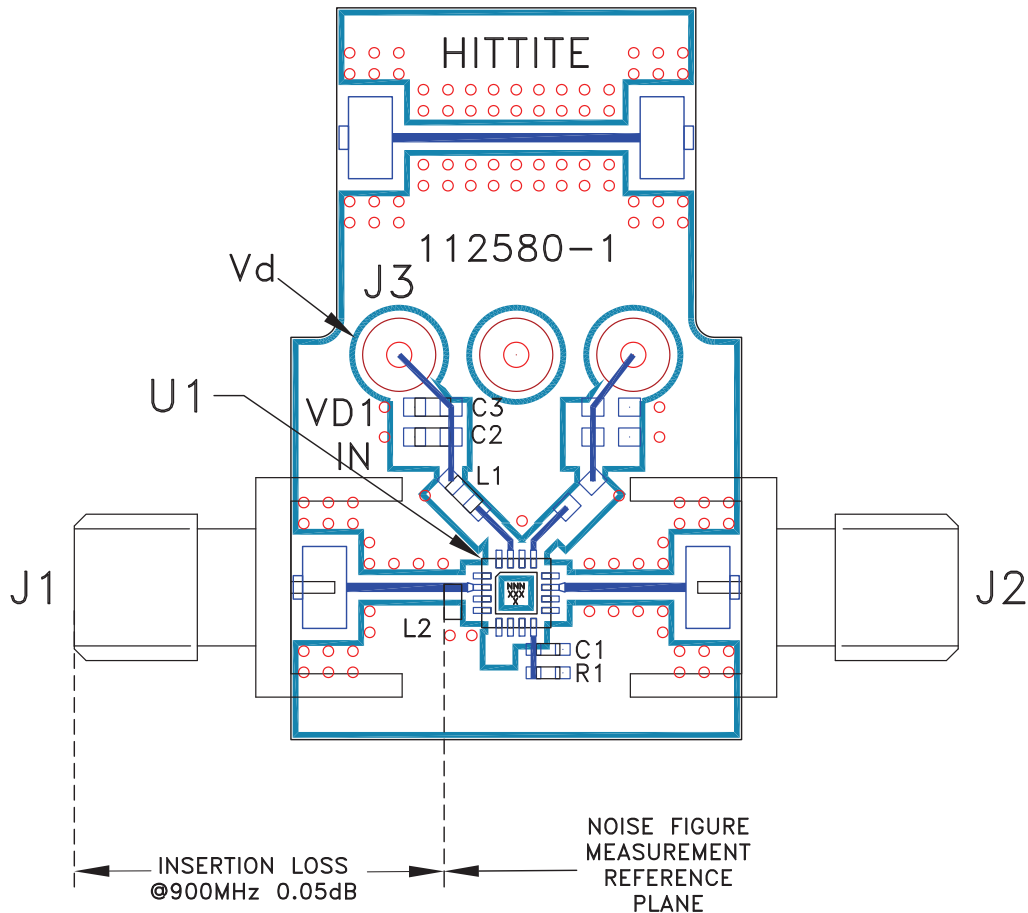
Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---------------------------------|----------|--|---------------------|
| 1, 3 - 5, 7, 9, 10, 12 - 14, 16 | N/C | No connection required. These pins may be connected to RF/DC ground without affecting performance. | |
| 2 | RFIN | This pin is matched to 50 Ohms. | |
| 6 | GND | This pin and ground paddle must be connected to RF/DC ground. | |
| 11 | RFOUT | This pin is matched to 50 Ohms. | |
| 8 | RES | This pin is used to set the DC current of the amplifier by selection of external bias resistor. See application circuit. | |
| 15 | Vdd | Power Supply Voltage. Choke inductor and bypass capacitors are required. See application circuit. | |

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB 118357 [1]

| Item | Description |
|---------|-------------------------------|
| J1, J2 | PCB Mount SMA RF Connector |
| J3, J4 | DC Pin |
| C1 | 10nF Capacitor, 0402 Pkg. |
| C2 | 1000 pF Capacitor, 0603 Pkg. |
| C3 | 0.47µF Capacitor, 0603 Pkg. |
| L1 | 18 nH, Inductor, 0603 Pkg. |
| L2 | 15 nH, Inductor, 0402 Pkg. |
| R1 | 3.92K Ohm Resistor, 0402 Pkg. |
| U1 | HMC617LP3(E) Amplifier |
| PCB [2] | 112580 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350.

The circuit board used in this application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.